REMARKS

Claims 1, 3, 5, 6, 8, 10, 15, 16, 18-20, 22-26, 28, 30-34, 36, 38, 45-50, 52-54, 56-74, and 76-85 are pending in this case. Claims 2, 4, 7, 9, 11-14, 17, 21, 27, 29, 35, 37, 39-44, 51, 55, and 75 have been canceled. Claims 2 and 20 are amended herein. No new matter has been added.

Double Patenting

The Examiner has provisionally rejected Claims 1, 3, 5, 6, 8, 10, 15, 16, 18-20, 23-26, 26, 30-34, 36, 38, 45, 46,48-50 and 56-61 as unpatentable on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 44-53 of copending U.S. Patent Application No. 08/483,938. Applicant notes that such application issued as U.S. Patent No. 7,038,290 ("the '290 patent") on May 2, 2006 and that the noted claims 44-53 correspond to claims 11-20 in the '290 patent. As such, Applicant will treat this as a nonstatutory obviousness-type double patenting rejection over claim 11-20 in the '290 patent. This rejection is respectfully traversed.

Present claim 1 is directed to a commercially mass-produced integrated circuit having a solid substrate of one conductivity type; a solid material pocket of a different conductivity type having a side surface and positioned on a selected top surface of the substrate; a signal-translating, electronic rectifying barrier located between the solid material pocket and the selected top surface of the substrate; and a solid state material region adjoining the solid substrate, the electronic rectifying barrier, and the side surface of said solid material pocket; wherein the solid state material region has a depth accuracy of better than 0.13 microns and is continuously and perfectly bonded metallurgically to all of the solid substrate, the solid material pocket, and the rectifying barrier, without

the presence of thermally and electrically insulating voids and microcracks that visible at 1,000 times magnification in interfacial bonding regions between the bonded device components.

Applicant points out that the present invention is directed to commercially mass-produced integrated circuit devices, which are different than, and on orders of magnitude more difficult to manufacture than, the solid state and active semiconductor devices of the '290 patent.

Specification

The Examiner has objected to the specification, alleging that Claim 20 recites "a terminal portion" in line 17, but that there is no antecedent basis for this term in the specification. Applicant respectfully submits that this objection is obviated in view of the amendment to the Specification.

Section 112, Second Paragraph Rejections (Indefiniteness)

The Examiner has rejected claims 3, 5, 20, 22-26, 28, 30-34, 36, 38 and 75 under 35 U.S.C. 112, second paragraph, as indefinite for the reasons set forth in the Office action. In view of the amendments made herein, Applicant respectfully submits that these rejections have been obviated.

Section 103 Rejections

The Examiner has rejected the pending claims under 35 U.S.C. 103(a) as unpatentable over U.S. Patent No. 4,916,716 ("Fenner") in view of U.S. Patent No. 3,341,754 ("Keller"). This rejection is respectfully traversed.

Applicant respectfully submits that the Examiner has failed to establish a prima facie case of obviousness. As set forth in

MPEP 706.02, in order to establish a prima facie case of obviousness, the Examiner must, among other things, provide an explanation as to why one of ordinary skill in the art at the time the invention was made would have been motivated to make the proposed invention. In the present case, the Examiner states that such motivation would be due to "meet basic design needs". However, Applicant respectfully submits that this is not accurate.

In this regard, Applicant points out that the device of Fenner is a Fig. 1 device is on a "Varactor Diode", which is an isolated, single unintegrated semiconductor diode device; it is not an integrated circuit as is the present invention. Further, in the present invention, all claims are directed to commercially mass-produced integrated circuits that call for extremely high dimensional precision and quality/yield to be commercially profitable and mass-producible. By contrast, Fenner claims only a single, isolated unintegrated semiconductor diode device having no other similar neighboring devices to isolate from. As such, motivation for combining the Fenner and Keller references cannot be found in simply meeting device design needs, and accordingly Applicant respectfully submits that the Examiner has not established a case of prima facie obviousness

Further, Applicants states that Fenner has a filing date more than eighteen years before the filing date of Applicant's U.S. Patent No. 3,430,109, which clearly discloses the use of oxide isolating grooves of various bottom shapes (see, for example, col. 2, lines 4-6), not just to guard the PN junction but, more importantly, to passivate the PN junction and to electrically isolate neighboring semiconductor devices on the same chip in an integrated circuit. Furthermore, the oxide groove has a cylindrically rounded bottom with zero bottom width

to maximize device miniaturization for oxygen masked diffusion process. The bottom of the oxide groove is down to 0.1 or near zero microns below the PN junction region. Fenner could not reliably and reproducibly mass-produce such devices, at least not in a commercially profitable manner. In order to achieve junction passivation, Applicant's oxide groove provides a rounded PN junction peripheral surface with a very large, surface or differential surface expansion for minimum leakage currents and maximum breakdown voltages. Only automatic groove forming methods with real time feed-back control, as disclosed in Applicant's '109 patent (see, for example, col. 2, lines 38-68), and in other patents, can produce smaller than submicron groove sizes, depths, and locations.

Furthermore, Applicant notes that, in his later U.S. Patent Application No. 154,300, filed June 18, 1971, and U.S. Patent No. 4,946,800, filed August 7, 1973, he disclosed that a rounded groove bottom reduces thermal mismatch stresses, and can, according to mobility tests, modify the stress and strain in silicon to improve device other performances. Applicant's U.S. Patent No. 3,585,714 patent deals in *Figs.* 6-7 hundreds of integrated devices on a single chip. Later patents are for new applications dealing with thousands, millions, and billions of physically integrated circuit devices on a single chip. The many, many components are electrically isolated from one another on a single chip by Applicant's unique oxide isolating grooves. The layer thicknesses, dimensions, radii, positions, depths, and stresses and strains in individual device components are orders of magnitude different from other devices. They are much more difficult to produce than those in Fenner's singular, un-integrated diodes. Applicant's '109 patent, which was filed in 1965, not only clearly discloses but, more importantly, explains in great details the minimum requirements, exact procedures, and

special automation equipment and technique to make the unique oxide-isolating grooves of zero bottom widths enabling highly miniaturized modern electronics

Moreover, Applicant notes that in Fenner (see Figure 1), whether the 4/3 rectifying barrier between layers 4 and 3 is a PN junction or Schottky barrier, the vertically flat or planar, non-curved, and unexpanded (certainly not "differentially surface expanded") junction peripheral surface was met by the equally vertically flat or planar and having non-expanded nor differentially expanded side surface on the pocket 7. Note that the metal or p-conductive layer 4 not only is flat-sided, and totally and irrelevantly above the weakly n-conductive semiconductor layer 3 by approximately 0.1 to 2 microns. See Fenner at col. 2, lines 55-60. The n-conductive semiconductor layer 3 is also flat-sided and totally above the hemi cylindrically "rounded" channel bottom of channel 7. Hence, the PN or Schottky rectifying barrier 4/3 is already over 0.1 and 2 microns above the "curved" portion of the channel bottom 7. The rectifying barrier was guarded but not passivated, and was easily contaminated by metals or dust particles to cause the same worldwide leakage current epidemic resulting in poor device yield and high cost, as explained in '109, at col. 4, line 56 to col. 5, line 41. Further, the flat-sided peripheral surface of the barrier has absolutely no surface expansion or differential surface expansion - another feature of Applicant's unique oxide grooves. Accordingly, the device of Fenner does not have passivated PN Junctions, expanded barrier peripheral surface, nor stress and strain relief for lack of curvature on the peripheral surface, and other features of Applicant's patented devices.

Applicant further notes that there is no other device to isolate from on the same chip. In the Fenner device, whether

the annular channel 7 shape is cylindrical, spherical, paraboroidal, conical, flat, or rounded (See Applicant's '109 patent at col. 2, lines 5-6) had nothing to do with the device breakdown voltage, leakage current, and device yield, and little to do with the overall diode size or miniaturization. Yet device miniaturization is extremely important in modern microelectronics where high miniaturization is absolutely necessary. Without device yield, there would be no products to sell. Without device miniaturization, there is no device miniaturization and, therefore, modern electronics, regardless of what the channel 7 shape, thickness, or location. The dimension of the various diode dimensions, the accuracy of the diode component dimensions, or the bonding qualities between the different diode component materials are then unimportant or irrelevant.

Applicant further notes that the use of intrinsic semiconductor material together with other doped semiconductor materials on the same semiconductor device was first specifically disclosed as Figures 3a and 3b in Applicant's aforementioned 154,30 application, over nine years before Fenner. But the use of intrinsic semiconductors was not claimed until Applicants' U.S. Patent Application Nos. 08/483,937 and 08/483,938, both filed on June 7, 1995, which generally claim the use of silicon on intrinsic silicon were for improving the impact resistance of these mixed intrinsic and doped semiconductor, single-material (e.g., silicon) devices. Still later, when the semiconductor industry was dead stuck at 100 nm devices because the very thin gate layers were always leaky, Applicant found that the new worldwide leakage currents arose from mismatches of thicknesses and thermal expansion coefficients of the gate layer relative to the substrate. The first of several proposed solutions was the use of silicon on

intrinsic semiconductor in "single-material circuits." Intel tried this approach with "intrinsic silicon sitting on top of silicon." The leakage current was drastically reduced by 1,000 times. The 90 nm barrier was broken, so was 65nm and possibly 35 nm. Applicant could not claim this early because the worldwide universal thin gate layer problem did not exist before about 2002.

Accordingly, Applicant respectfully submits that Fenner does not set forth an enabling disclosure of the subject matter claimed in the present application, as supported by Applicant's discussion of the development of the art in this field, specifically with respect to the use of unique materials thicknesses, configurations, and thermal mismatch coefficients, radii of curvature, processing steps, and equipment for making a commercially mass-producible and profitable integrated circuits for the new technologies listed below.

Accordingly, Applicant respectfully submits that the withdrawal of the outstanding rejections under Section 103 is appropriate and is respectfully requested.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance, and an early notice to that effect is respectfully requested.

Please direct any questions concerning this Response to Applicant's undersigned representative, who can be reached directly at (610) 869-6302.

Respectfully submitted,
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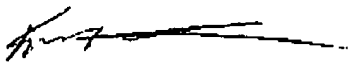

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